IN THE CLAIMS

Claim 1 (currently amended): A circuit adapted to generate a tail current for a main amplifier stage, comprising:

a ~~scaled~~ master stage circuit;

a balanced stage circuit;

the ~~scaled~~ master stage circuit responsively coupled to the balanced stage circuit,

the ~~scaled~~ master stage having a predetermined offset operable to force a given tail current to the balanced stage circuit and a main reader amplifier; and

the balanced stage circuit comprising at least one bi-polar and MOS transistor differential pair adapted to provide a balanced offset to the master stage circuit.

Claim 2 (currently amended): The circuit adapted to generate a tail current for a main amplifier stage of Claim 1, wherein ~~a~~ said main reader amplifier is in combination with the circuit adapted to generate a tail current for the main amplifier stage.

Claim 3 (original): The circuit of Claim 1, wherein the bi-polar transistors comprise NPN transistors and the MOS transistors comprise NMOS transistors.

Claim 4 (original): The circuit of Claim 1, wherein the bi-polar transistors comprise PNP transistors and the MOS transistors comprise PMOS transistors.

Claim 5 (original): The circuit of Claim 1, being adapted to achieve a low, low-corner –3dB frequency and low noise threshold compared to an all bipolar differential pair.

Claim 6 (currently amended): The circuit adapted to generate a tail current for a main amplifier stage of Claim 1, wherein the tail current of the ~~scaled~~ master stage circuit is adapted to drive semiconductor devices in a reader amplifier.

Claim 7 (original): Bias circuitry for a reader amplifier, comprising:

a master transconductance (gm) stage configured as a scaled reader amplifier;

a balanced stage circuit; and

the scaled reader amplifier responsively coupled to the balanced stage circuit.

the scaled reader amplifier operable to provide a tail current for the balanced stage circuit and a reader amplifier.

Claim 8 (original): The bias circuitry for a reader amplifier of Claim 7, having an output matching an absolute current as a function of a predetermined voltage input offset.

Claim 9 (original): The bias circuitry for a reader amplifier of Claim 8, wherein the predetermined voltage input offset is about 50 mV.

Claim 10 (original): The bias circuitry for a reader amplifier of Claim 7, wherein the master transconductance stage has a precise gm independent of processing variations.

Claim 11 (original): A circuit arrangement for providing a tail current to an amplifier, comprising:

a scaled master differential stage;

a balanced stage circuit comprising at least one bi-polar and MOS transistor differential pair adapted to provide a balanced offset to the scaled master differential stage;

the scaled master differential stage having a given offset adapted to force a given tail current.

Claim 12 (currently amended): The circuit arrangement <u>for providing a tail current to an amplifier</u> of Claim 11 in combination with a main reader amplifier.

Claim 13 (currently amended): The circuit arrangement of Claim 11, wherein said at least one bipolar transistor is responsively coupled to a magneto-resistive element and at least one MOS transistor is responsively coupled to an AC-coupling capacitor.

Claim 14 (original): The circuit arrangement of Claim 11 wherein the bipolar transistor comprises an NPN transistor and the MOS transistor comprises an NMOS transistor.

Claim 15 (original): The circuit arrangement of Claim 11, wherein the bipolar transistor comprises a PNP transistor and the MOS transistor comprises a PMOS transistor.

Claim 16 (original): A tail current generator circuit, comprising:

a master transconductance stage;

a balanced offset stage including at least one bipolar-MOS differential transistor pair adapted to provide a balanced offset to the master transconductance stage;

the master transconductance stage adapted to set a precise transconductance of the bipolar-MOS differential transistor pair; and

the tail current generator circuit responsive to the master transconductance stage and operable to provide an output which matches an absolute current as a function of a predetermined voltage input offset.

Claim 17 (original): The tail current generator circuit of Claim 16, wherein the bipolar transistor comprises an NPN transistor and the MOS transistor comprises an NMOS transistor.

Claim 18 (original): The tail current generator circuit of Claim 16, wherein the bipolar transistor comprises a PNP transistor and the MOS transistor comprises a PMOS transistor.

Claim 19 (original): A method of generating a tail current for an amplifier, comprising the steps of:

adapting a differential, scaled master stage to accept a balanced offset;

generating a current by a feedback arrangement in the differential, scaled master stage;

scaling the current derived in the differential, scaled master stage; and

providing the scaled current as the tail current for an amplifier.

Claim 20 (original): The method of generating a tail current of Claim 19, further comprising using a bipolar/MOS differential pair in a balanced stage circuit to provide the balanced offset.

Claim 21 (currently amended): The method of generating a tail current ~~in~~ of Claim 20, wherein said at least one bipolar transistor is responsively coupled to a magneto-resistive element and at least one MOS transistor is responsively coupled to an AC-coupling capacitor.

Claim 22 (original): The method of generating a tail current for an amplifier of Claim 19, wherein the differential, scaled master stage is a scaled version of a main reader amplifier input stage.

Claim 23 (original): The method of generating a tail current of Claim 19, for use as a bias circuit in a reader amplifier of a disk drive system.